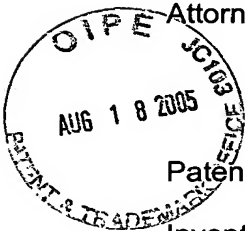


Patent No. 6,879,176  
Request for Cert. of Correction dated August 16, 2005  
Attorney Docket No. 1880-031248

10/701226

COPY



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent No. : 6,879,176 B1 Confirmation No. 5253  
Inventor : Robert J. HILLARD  
Issued : April 12, 2005  
Title : Conductance-Voltage (GV) Based Method For  
Determining Leakage Current in Dielectrics  
Examiner : Jermele M. Hollington  
Customer No. : 28289

Certificate  
AUG 24 2005  
of Correction

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT  
FOR PTO MISTAKE (37 C.F.R. 1.322(a))

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

ATTENTION: Decision and Certificate of Correction Branch  
Patent Issue Division

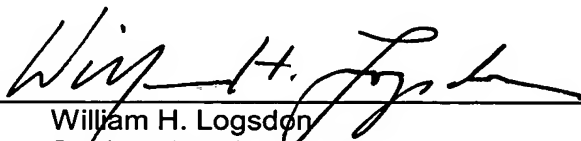
Sir:

In accordance with 35 U.S.C. §254, we attach hereto Form PTO/SB/44 and a copy of proof of PTO's error and request that a Certificate of Correction be issued in the above-identified patent. The following error appears in the patent as printed:

Face of Patent, See Item (57) ABSTRACT, line 2, "can be determining" should read -- can be determined --.  
(See application, page 11, Abstract, lines 4 - 5.)

Respectfully submitted,

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## UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO. : 6,879,176 **B1**  
DATED : April 12, 2005  
INVENTOR(S) : Hillard

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Face of Patent, See Item (57) ABSTRACT, line 2, "can be determining"  
should read -- can be determined --.

{W0206716.1}

MAILING ADDRESS OF SENDER:

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PATENT NO. 6,879,176

No. of additional copies



This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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ALC 2 4 2005



## CONDUCTANCE-VOLTAGE (GV) BASED METHOD FOR DETERMINING LEAKAGE CURRENT IN DIELECTRICS

### BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to determining the quality of a dielectric on a semiconductor wafer.

[0003] 2. Description of Related Art

[0004] A semiconductor wafer utilized to form integrated circuits typically includes a dielectric overlaying a top surface of the semiconductor wafer. Prior to processing the semiconductor wafer to form arrays of integrated circuits thereon, it is desirable to determine various parameters associated with the dielectric. Two such parameters include equivalent oxide thickness (EOT) and leakage current ( $I_{leak}$ ).

[0005] Heretofore, separate instrumentation and probes were utilized to measure these parameters. However, the use of separate instrumentation and probes increases the difficulty, cost and throughput of such measurements. In addition, the measurement of leakage current heretofore required the use of two frequencies.

[0006] It is, therefore, desirable to overcome the above problems and others by providing a method wherein leakage current can be determined utilizing a single frequency. It is also desirable to provide a method where measurements utilized to determine leakage current of a dielectric can also be utilized to derive other parameters of interest for the dielectric.

### SUMMARY OF THE INVENTION

[0007] The invention is a method of determining leakage current of a dielectric overlaying a semiconductor wafer. The method includes providing a semiconductor wafer having a dielectric overlaying at least part of the semiconductor wafer and providing a probe having an elastically deformable conductive tip. The probe tip is caused to move into contact with the dielectric and a DC voltage having an AC voltage superimposed thereon is applied between the probe tip and the semiconductor wafer. The DC voltage is then swept from a first DC voltage toward a second DC voltage. Phase angles between the AC voltage and an AC current flowing through the dielectric in response to the AC voltage during the sweep of the DC voltage are acquired. Changes in the conductance of the semiconductor wafer and the dielectric as a function of changes in the voltage



## CONDUCTANCE-VOLTAGE (GV) BASED METHOD FOR DETERMINING LEAKAGE CURRENT IN DIELECTRICS

### ABSTRACT OF THE DISCLOSURE

A leakage current of a dielectric overlaying a semiconductor wafer can be determined by moving a conductive probe into contact with the dielectric and applying an electrical stimulus, in the form of a fixed amplitude, fixed frequency AC voltage superimposed on a DC voltage which is swept from a starting voltage towards an ending voltage, between the probe tip and the semiconductor wafer. Conductance values associated with the dielectric and the semiconductor wafer can be determined from phase angles between the AC voltage and an AC current resulting from the applied AC voltage during the sweep of the DC voltage. The leakage current of the dielectric can then be determined from the thus determined conductance values.